# TN2115S2 Specification

**8 MHz ARM Cortex-M0, 32KB FLASH ROM, 8KB RAM, 13 GPIOs, SWD, Passive Execution**
**300mW NFC Energy Harvesting, 2KB EEPROM, I2C, SPI, Adaptive Harvester**

## 1. Features

- **MCU for Passive Operation**
  - 32bit ARM Cortex-M0
  - Up to 12MHz clock
  - On-chip RC clock
  - On-chip SWD debug interface
  - 13 GPIOs
  - NFC OTA update capability
  - Run/ Sleep Modes
  - SW NFC protocol stack
  - Execute using harvested energy
  - Passive computing/sensing/actuating
- **SW-configurable NFC Interface**
  - 106kbps data rate
  - 2KB on-chip EEPROM
  - Support TYPE2 tag interface
  - Support TYPE4 tag interface
  - Support user-defined protocol
  - 4/7/10 Bytes UID, reconfigurable
- **Efficient Energy Harvesting**
  - Optimized NFC AFE
  - Up to 300mW harvested power
  - Power the entire IC passively
  - Power the host devices passively
  - Single-chip computing/powering
- **High-speed Serial Data Bus**
  - I2C slave, up to 400kbps
  - SW I2C&SPI master
  - Interrupt upon RX/TX
- **Versatile Storage Options**
  - 32KB system FLASH
  - 8KB system RAM
  - 2KB data EEPROM
- **Effective Power Management**
  - Harvesting output: Raw/3.3V/1.8V
  - Adaptive harvesting: power + stability
  - Interfacing with super capacitors
  - NFC data communication protection
  - Wide input: 2.3V – 15V
- **Low Power Consumption**
  - 500uA in MCU sleep state
  - <3mA in run state
  - 600uA average in typical scenarios

# 2. General Description

## 2.1. Summary

TN2115S2 is a NFC passive MCU, which integrates an ISO14443A-compliant NFC tag interface. The MCU is designed with Chivotech's exclusive TurboNFC technology that offers high-efficient energy harvesting. TN2115S2 is able to harvest up to 300mW power when working with typical NFC-equipped smartphones. Such amount of power not only allows TN2115S2 to run at full speed passively, but also is able to drive externally connected devices like sensors, displays, and actuators.

The core of TN2115S2 is an ARM CORTEX-M0 running up to 12MHz. On-chip high-speed serial bus interfaces, peripherals, GPIOs, and abundant storage options including RAM, FLASH, and EEPROM are connected to the core through AHB. The internal FLASH stores system library and user's code and data. An on-chip EEPROM is also provided to store user data or system configurations. The typical current draw of TN2115S2 is below 1mA.

Chivotech's advanced NFC architecture grants the user the ability to easily interface user code and 3rd libraries to the NFC functionalities. It also enables non-standard, user-defined NFC protocols to be easily implemented on TN2115S2. TN2115S2 also includes an adaptive harvesting controller. Loads with super low ESR, such as large supercapacitors and motors can be directly connected to the harvesting output without collapsing the NFC RF field.

TN2115S2's excellent harvesting capability and versatility is well suited for mobile devices, smart home devices, and IoT devices. For example, smartlocks with TN2115S2 integrated can work without batteries, as the energy for the lock/unlock actions can be provided wirelessly by smartphones.

## 2.2. Characteristics

| NAME | VALUE |
|---|---|
| MCU CLOCK RATE | 6MHz – 12MHz |
| MCU FLASH | 32KBytes |
| MCU RAM | 8KBytes |
| EEPROM | 2KByte |
| GPIOS | 13Configurable GPIO |
| NFC DATA RATE | 106Kbps |
| HARVESTING POWER | Up to 300mW,typically 60mW – 150mW |
| HARVESTING OUTPUT | RAW/3.3V/1.8V |
| INPUT VOLTAGE | 2.3V – 15V |
| CURRENT DRAW | 600uA typically |

## 2.3. Typical Applications

TN2115S2's typical applications include smartcards, wearable devices, and IoT devices. The MCU offers NFC data transfer and wireless powering functions in both battery and battery-less modes. Exemplary applications include Eink price tags, Bluetooth-enabled/display-enabled/biometric-enabled smartcards, smartlocks, sensors, and smartphone accessories.

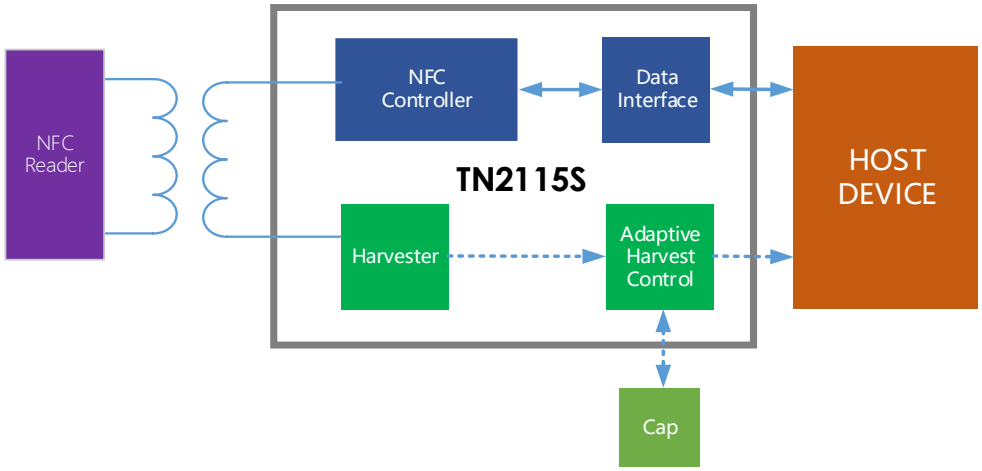



Fig. 1 Application Diagram

## 2.4. Footprint and Marking

| MARKING | FOOTPRINT | DESCRIPTION | VERSION |
|---|---|---|---|
| TN2115SX | QFN40 | 5mm x 5mm, 0.55mm Height，leadless，40pins | V1.0 |

Tab. 1 Footprint

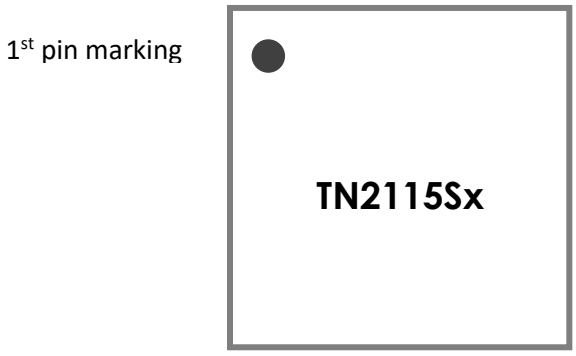
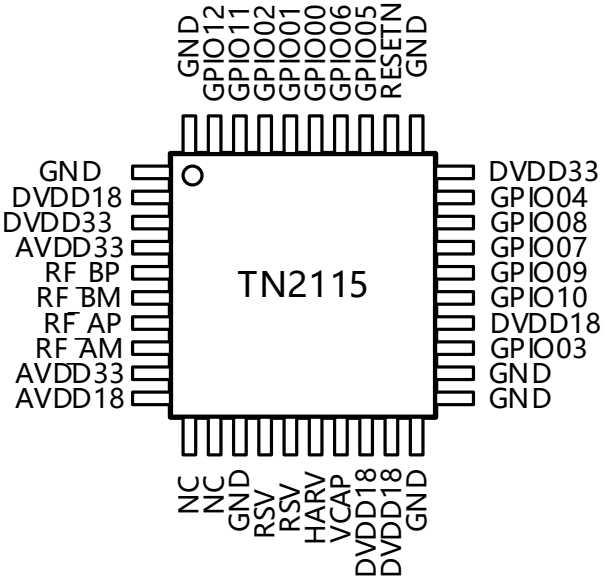



Fig. 2 Marking

## 2.5. Security

- On-chip FLASH password lock to prevent accidental write operations
- On-chip FLASH readout protection unit
- NFC Security level is fully controlled by the MCU
  - Reconfigurable 4/7/10 Byte ID, controller by the MCU
  - SW security measures inside MCU for low-cost, non-security-sensitive applications
  - External HW security element for maximum security insurance (passively powered)
- NFC tag memory access model is controlled by the MCU
  - NFC shutdown
  - Memory non-visible
  - Memory read-only
  - Memory write-only
  - Memory full access
  - Volatile or non-volatile

# 3. Pin Definitions

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5. Fig. 3 TN2115S2 pin definitions

| PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | GND | Ground | GND |
| 2 | DVDD18 | Power | 1.8v input, must connect with avdd18 |
| 3 | DVDD33 | Power | 3.3V digital power in |
| 4 | AVDD33 | Power | 3.3v LDO output, must connect with a 0.47uf capacitor |
| 5 | RF_BP | Analog/in | NFC antenna B |
| 6 | RF_BM | | |
| 7 | RF_AP | | |
| 8 | RF_AM | Analog/in | NFC antenna A |
| 9 | AVDD33 | Power | 3.3v LDO output, must connect with a 0.47uf capacitor |
| 10 | AVDD18 | Power | 1.8v LDO output, must connect with a 0.1uf capacitor |
| 11 | NC | - | Must left unconnected |
| 12 | NC | - | MUST LEFT UNCONNECTED |
| 13 | GND | Ground | GND |
| 14 | RSV | Reserved | MUST LEFT UNCONNECTED |
| 15 | | | |
| 16 | HARV | Harvester out | Harvesting output, not regulated, not load protected |
| 17 | VCAP | Harvester out | Adaptive harvesting output, not regulated |

| | | | |
|---|---|---|---|
| 18 | DVDD18 | Power | 1.8v input, must connect with avdd18 |
| 19 | DVDD18 | Power | 1.8v input, must connect with avdd18 |
| 20 | GND | Ground | GND |
| 21 | GND | Ground | GND |
| 22 | GND | Ground | GND |
| 23 | GPIO03 | Digital/in/out | GPIO. Default: SWDIO，see registers for configuration |
| 24 | DVDD18 | Power | 1.8v input, must connect with avdd18 |
| 25 | GPIO10 | Digital/in/out | GPIO. See registers for configuration |
| 26 | GPIO09 | Digital/in/out | GPIO. See registers for configuration |
| 27 | GPIO07 | Digital/in/out | GPIO. See registers for configuration |
| 28 | GPIO08 | Digital/in/out | GPIO. See registers for configuration |
| 29 | GPIO04 | Digital/in/out | GPIO. Default: SWCLK，see registers for configuration |
| 3 | DVDD33 | Power | 3.3V digital power in |
| 31 | GND | Ground | GND |
| 32 | RESETN | Digital/in | Chip reset pin, active low |
| 33 | GPIO05 | Digital/in/out | GPIO. See registers for configuration |
| 34 | GPIO06 | Digital/in/out | GPIO. See registers for configuration |
| 35 | GPIO00 | Digital/in/out | GPIO. |
| 36 | GPIO01 | Digital/in/out | GPIO. |
| 37 | GPIO02 | Digital/in/out | GPIO. |
| 38 | GPIO11 | Digital/in/out | GPIO/I2C_SCL，see registers for configuration |
| 39 | GPIO12 | Digital/in/out | GPIO/I2C_SDA，see registers for configuration |
| 40 | GND | Ground | GND |

6.

7. Tab. 2 Pin definitions

# 8. Electrical Characteristics

## 8.1. Absolute Maximum Ratings

| Ratings | Min | Max | Unit | Note |
|---|---|---|---|---|
| Working Temperature | -40 | +125 | ℃ | |
| Hi-volt Analog IO Voltage | -0.7 | 18 | V | Include RF_CM，RF_CP，VHARV，VCAP |
| Lo-volt Analog IO Voltage | Vss-0.7 | 5 | V | All other analog IOs |
| Digital IO Voltage | -0.7 | 4.2 | V | All digital IO |
| ESD | | 3 | KV | |
| Hi-volt Analog IO Current | | 100 | mA | Include VHRAV，VCAP |
| Lo-volt Analog IO Current | | 50 | mA | Include AVDD3V3，AVDD1V8，VREF1P2 |
| Digital IO Current | -20 | 20 | mA | |

Tab. 3 Absolute Maximum Ratings

## 8.2. Recommended Working Conditions

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Working Temperature | | -40 | | +85 | ℃ |
| $H_A$ | RF Field Strength | | TBA | TBA | TBA | A/M |

Tab. 4 Recommended Working Conditions

## 8.3. Electrical Parameters

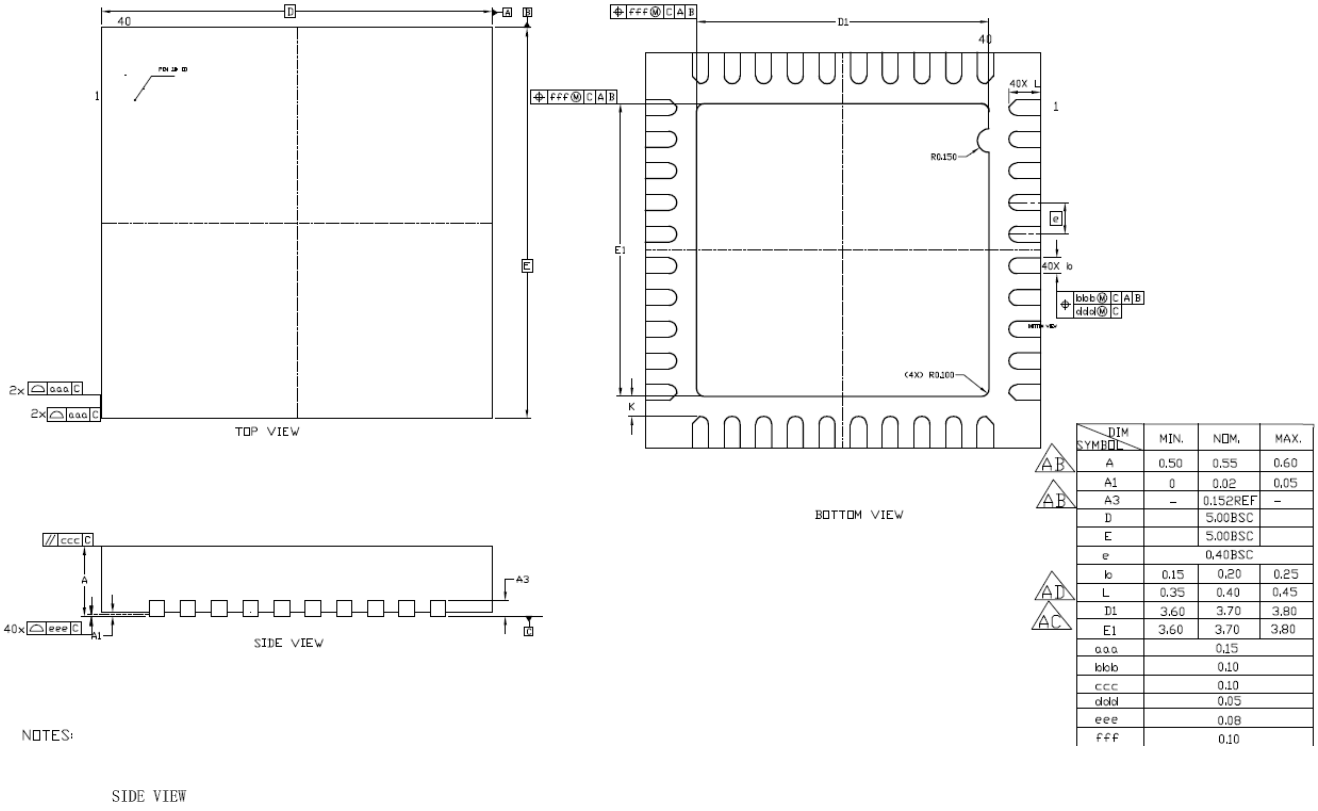
| Parameter | Conditions | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| **RF Section** | | | | | |
| Antenna input frequency | | | 13.56 | | MHz |
| Input parasitic Capacitance | RFC pin | | | 10 | pF |
| **On-chip RC Oscillator** | | | | | |
| Output Frequency VBG = 500mV | OSCTRIM = 1 | | 5.9 | | Mhz |
| | OSCTRIM = 2 | | 6.4 | | Mhz |
| | OSCTRIM = 3 | | 6.9 | | Mhz |
| | OSCTRIM =4 | | 7.2 | | Mhz |
| | OSCTRIM = 5 | | 7.7 | | Mhz |
| | OSCTRIM = 6 | | 8.1 | | Mhz |
| | OSCTRIM = 7 | | 8.5 | | Mhz |
| | OSCTRIM = 8 | | 8.8 | | Mhz |
| | OSCTRIM = 9 | | 9.2 | | Mhz |
| | OSCTRIM = 10 | | 9.6 | | Mhz |
| | OSCTRIM = 11 | | 9.9 | | Mhz |
| | OSCTRIM = 12 | | 10.3 | | Mhz |
| | OSCTRIM = 13 | | 10.7 | | Mhz |
| | OSCTRIM = 14 | | 11 | | Mhz |
| | OSCTRIM = 15 | | 11.3 | | Mhz |
| **Current Consumption** | | | | | |
| Run State Current | IO output = 0 OSCTRIM = 7 T = 25C | | 2500 | | uA |
| Sleep State Current | IO output = 0 OSCTRIM = 7 T = 25C | | 500 | | uA |

| | | | | | |
|---|---|---|---|---|---|
| **MCU Timings** | | | | | |
| Cold boot time | R = 10K<br>C = 0.1uF<br>T = 25C | 1 | 2 | 3 | mS |
| Sleep to Run Wakeup Time | T = 25C | | | 5 | uS |
| **Storage** | | | | | |
| FLASH program cycles | T = 25C | | 1000 | | cycles |
| FLASH data retention | T = 25C | | 10 | | years |
| EEPROM program cycles | T = 25C | | 1000 | | cycles |
| EEPROM data retention | T = 25C | | 10 | | years |
| **Digital Input IOs** | | | | | |
| Input high voltage | T = 25C | 0.7*AVDD33 | | | V |
| Input low voltage | T = 25C | | | 0.3*AVDD33 | V |
| Pin leakage current | | | | TBA | uA |
| **Digital Ouput IOs** | | | | | |
| Output high voltage | I = 2mA | 0.95*AVDD33 | | | V |
| Output low voltage | I = 2mA | | | 0.1*AVDD33 | |
| Output Current | Vio > 0.95*AVDD33 | TBA | | | mA |

Tab. 5 Electrical Parameters

# 9. Footprint and Drawings

## QFN40 Footprint




| DIM SYMBOL | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | – | 0.152REF | – |
| D | | 5.00BSC | |
| E | | 5.00BSC | |
| e | | 0.40BSC | |
| b | 0.15 | 0.20 | 0.25 |
| L | 0.35 | 0.40 | 0.45 |
| D1 | 3.60 | 3.70 | 3.80 |
| E1 | 3.60 | 3.70 | 3.80 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

Fig. 4 Drawings

# 10. Revision Information

*V1.01 revision : Revised pin definition and removed unnecessary pins*

V1.02 revision : Removed redundant and unnecessary descriptions, revised IC parameters, updated footprint

*V1.03 revision : Company name change reflection. Fixed pin definitions in chapter 3.*

*V1.04 revision : Fixed IC broken models*

*V1.05 revision : Removed incorrect UART descriptions*